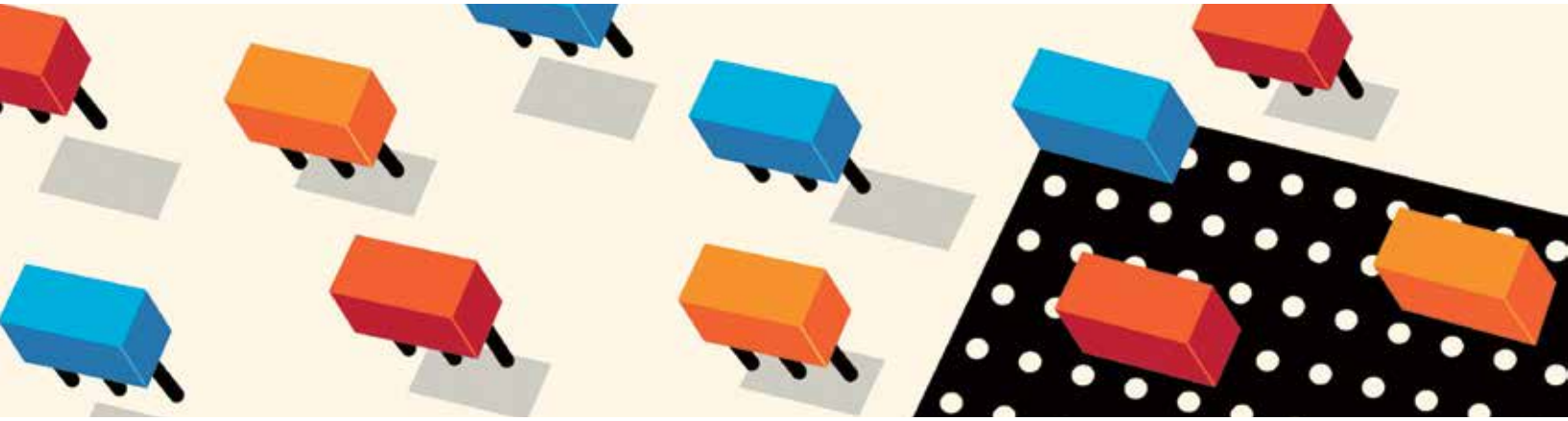


Harry Campbell

Moore's law: Repeal or renewal?

Economic conditions could invalidate Moore's law after decades as the semiconductor industry's innovation touchstone. The impact on chip makers and others could be dramatic.

Harald Bauer, Jan Veira, and Florian Weig

The global semiconductor industry has recorded impressive achievements since 1965, when Intel cofounder Gordon Moore published the observation that would become the industry's touchstone. Moore's law states that the number of transistors on integrated circuits doubles every two years, and for the past four decades it has set the pace for progress in the semiconductor industry. The positive by-products of the constant scaling down that Moore's law predicts include simultaneous cost declines, made possible by fitting more transistors per area onto silicon chips, and performance increases with regard to speed, compactness, and power consumption. As a result, semiconductor-enabled products today play integral roles in virtually every aspect of modern life.

In this article, we will examine the technologies that aim to extend the life of Moore's law and model their impact on four likely future scenarios for the industry. Obviously, there are many factors in play, but we believe the economics of continued advances in performance could eventually disrupt the companies competing in the business today.

How Moore's law drives the global economy

Adherence to Moore's law has led to continuously falling semiconductor prices. Per-bit prices of

dynamic random-access memory chips, for example, have fallen by as much as 30 to 35 percent a year for several decades.

As a result, Moore's law has swept much of the modern world along with it. Some estimates ascribe up to 40 percent of the global productivity growth achieved during the last two decades to the expansion of information and communication technologies made possible by semiconductor performance and cost improvements.

Enabled by constant technological innovation

The law retains its predictive power because of constant improvements in production technology, which are driven by the industry's "global semiconductor road maps." These describe the progress required for the continuation of Moore's law. This cycle of innovation began with the production of the first semiconductor circuits, then continued unabated with the introduction of clean-room technology in the 1970s, and it is sustained by today's fabrication

Exhibit 1

Four kinds of innovation should drive growth in semiconductors.

	Description	Examples	Expected timeline	Key challenges
1 More Moore (scaling)	Further development of CMOS[1] technologies (silicon based) to increase performance and reduce costs via geometrical and design scaling	• Extreme-ultraviolet (EUV) lithography • Multicore system-on-a-chip (SOC) architectures	• Short to midterm	• Large financial investment needed (eg, EUV) • Some technologies are not yet available or are close to physical limits
2 Wafer-size increases (maximize productivity)	Increase productivity by introducing larger wafer size: 450 millimeters (mm) for leading edge, 300mm for lagging edge	• Shift of analog and power products to 300mm	• Ongoing for 300mm • Midterm for 450mm	• Large financial investment necessary
3 More than Moore (functional diversification)	Added functionality (eg, interfaces, nondigital components) in package (SIP[2]) or chip (SOC), not scaling with Moore's law	• Integration of power management and wireless baseband in application processor	• Short to midterm	• Development of new technologies needed • New capabilities and skills needed
4 Beyond CMOS (new technologies)	Use of new technologies and materials for information processing and switching	• Spintronics • Carbon nanotubes • Quantum computing	• Mid- to long term	• Technologies are in early stages of development • Commercial scalability of technologies pending

[1]Complementary metal-oxide semiconductor.
[2]System in a package.

Source: International Technology Roadmap for Semiconductors; ObservatoryNANO; McKinsey analysis

plants, or fabs, often considered the most advanced production facilities ever built.

Whether Moore's law will apply in the future depends on technological developments, with one of the most critical areas of innovation involving lithography tools, especially extreme-ultraviolet (EUV) lithography technology. EUV uses short-wavelength light sources to scale feature sizes below 10 nanometers (nm). (See deep dive, "Innovations in lithography and EUV.")

However, lithography is not the only potential source of productivity improvements in semiconductor manufacturing; other cost-saving and performance-improvement methods are also in play. Companies are working toward larger semiconductor wafer sizes (see deep dive, "Transitioning to 450mm wafers") and will likely introduce new materials into chip designs. In fact, we see four types of innovation with the potential to propel semiconductor industry growth and performance improvements (Exhibit 1).

From a technological perspective, these innovations make progress based on Moore's law—smaller feature sizes and improved performance—a viable assumption for at least the next five to ten years. Our analysis of leading-edge chip technologies also supports a continuation of Moore's law from a demand perspective. While McKinsey research suggests that the number of leading-edge market segments will decline, those remaining, such as in mobile applications, should grow strongly, providing sufficient demand for high-end technologies.

Will economics doom Moore's law?

While the trends appear positive for the continued applicability of Moore's law from a technological perspective, economics could prove its undoing. Recent developments indicate that the economics of continued miniaturization could break down as cost-per-transistor reductions flatten for nodes with feature sizes below 28nm.

The culprits are the rapidly rising costs associated with technology development and the capital equipment needed to produce next-generation nodes. These cost increases are largely driven by the extreme investments required for leading-edge lithography technologies and the process complexity inherent in the double-patterning and multipatterning approaches used for nodes at 32nm and 28nm and below.

A McKinsey analysis shows that moving from 32nm to 22nm nodes on 300-millimeter (mm) wafers causes typical fabrication costs to grow by roughly 40 percent. It also boosts the

While the trends appear positive for the continued applicability of Moore's law from a technological perspective, economics could prove its undoing.

Exhibit 2

Several scenarios offer snapshots of the industry's potential evolution.

Performance[2] increases through node scaling[3]	Cost improvements through node scaling[1]: Continue	Cost improvements through node scaling[1]: Stop
Continue	**I Moore's law continues** • Node scaling continues • Leading-edge segments continue to consolidate to absorb capital expenditure • End-market demand is stable	**III Cost improvements end but performance increases continue[4]** • Node scaling continues for segments that value performance[5] • Leading-edge segments continue to consolidate to absorb capital expenditure • Demand is at risk due to a lack of continuous cost decreases
Stop	**II Performance increases end but cost improvements continue[4]** • Node scaling continues • Leading-edge segments continue to consolidate to absorb capital expenditure • Demand is at risk due to a lack of continuous performance increases	**IV Moore's law ends** • Industry becomes commoditized • Lagging-edge players have a chance to catch up • Demand is disrupted due to negligible improvements in cost and performance

[1]Additional cost improvements (eg, due to wafer-size increases, yield improvements, and equipment effectiveness) are independent of this.
[2]Increase of absolute or relative performance (ie, performance per power consumption).
[3]Additional performance increases (eg, due to "more than Moore" effects and software) are independent of this.
[4]These scenarios can only be transition stages for the industry; in the long term, they do not offer a stable equilibrium from an economic perspective.
[5]Examples include central processing units or wireless.

costs associated with process development by about 45 percent and with chip design by up to 50 percent. These dramatic increases will lead to process-development costs that exceed $1 billion for nodes below 20nm. In addition, the state-of-the art fabs needed to produce them will likely cost $10 billion or more. As a result, the number of companies capable of financing next-generation nodes and fabs will likely dwindle.

Exploring four potential scenarios

When assessing the industry's future, leaders may find it helpful to consider four scenarios reflecting uncertainties about the viability of tomorrow's semiconductor cost and performance improvements (Exhibit 2).

Each scenario reflects different assumptions regarding the sources of differentiating innovation, the potential for commoditization, and shifts

in customer demand; each also takes into account the industry's dynamics, return on invested capital (ROIC), and ability to capture value (Exhibit 3). Take, for example, the scenario in which cost improvements end but performance increases continue. Node scaling would continue, but only for players that seek higher performance and are willing to pay for it. Industry participants would see little increased risk of commoditization, but

Exhibit 3

Different assumptions underlie each scenario.

	I Moore's law continues	II Performance increases end	III Cost improvements end	IV Moore's law ends
Source for differentiating innovation	• Node scaling for cost and performance	• Node scaling for cost • Other innovations[1] for performance	• Node scaling for performance • Other innovations[1] for cost	• Other innovations[1] for cost and performance
Increased commoditization risk	• No, node scaling differentiates via performance	• Yes, lack of "automatic" performance differentiation	• No, node scaling differentiates via performance	• Yes, lack of "automatic" performance differentiation
Increased risk for end-customer demand[2]	• No	• Yes, given lack of continuous performance increases	• Yes, given lack of cost declines	• Yes, given lack of cost and performance improvements
Industry dynamics	← Oligopoly, with few remaining leading-edge players with their own fabs and consolidation of fabless players given exploding capital costs →			• Large players aim to dominate commodity market via scale effects • Lagging-edge players have the ability to catch up
Return on invested capital in industry	← Declining because of exploding capital required for smaller nodes →			• Improving because there is no need for capital expenditure/ R&D spending for new nodes
Industry ability to capture value	• Improved because of market power of a few players and stable demand	At risk from demand disruption →		• Highly at risk given commoditization and demand disruption

[1]Examples include innovative chip design and software.
[2]Does not consider end-customer demand disruptions happening independent of a semiconductor-related "trigger" (eg, lack of end-customer demand for better smartphone performance).

DEEP DIVE

Innovations in lithography and EUV

Lithography has enabled the semiconductor industry to achieve continually smaller nodes for the past 25 years. As argon fluoride (ArF) immersion lithography reached its critical limit, the industry introduced double and multipatterning, which made scaling to 32 nanometers (nm) and below possible. Double and multipatterning enables further node scaling by overlaying several lithography steps to enhance feature density. Multipatterning was first used for 32nm and 28nm nodes and could enable the industry to scale nodes down to 14nm and even smaller.

However, complex lithography approaches like multipatterning carry a high price. As a result, the percentage of corporate capital spending allocated to lithography will rise to an estimated 24 percent for 2010–15 from an average of less than 20 percent in 2000–05. What's more, per-layer costs and accompanying complexity levels are exploding for double and multipatterning. For instance, moving to 22nm with double patterning, from 32nm ArF immersion without it, could double the number of process steps per layer, depending on the product, and raise costs per layer by 50 percent. This trend could lead to a breakdown of Moore's law as the cost advantages that traditionally come with scaling disappear.

There is, however, a technological innovation that could overcome these challenges, extreme-ultraviolet (EUV) lithography. This technology uses new light sources with a wavelength of 13.5nm. The industry expects EUV to reduce per-layer costs because fewer steps will be needed compared with double or multipatterning. Double patterning, for example, can require more than 30 patterning steps per layer, but EUV will likely need just 10, with resulting cost-per-layer advantages estimated to be as high as 35 percent. In addition, EUV promises to deliver node sizes of 10nm and below because of the smaller wavelength of the lithography tools.

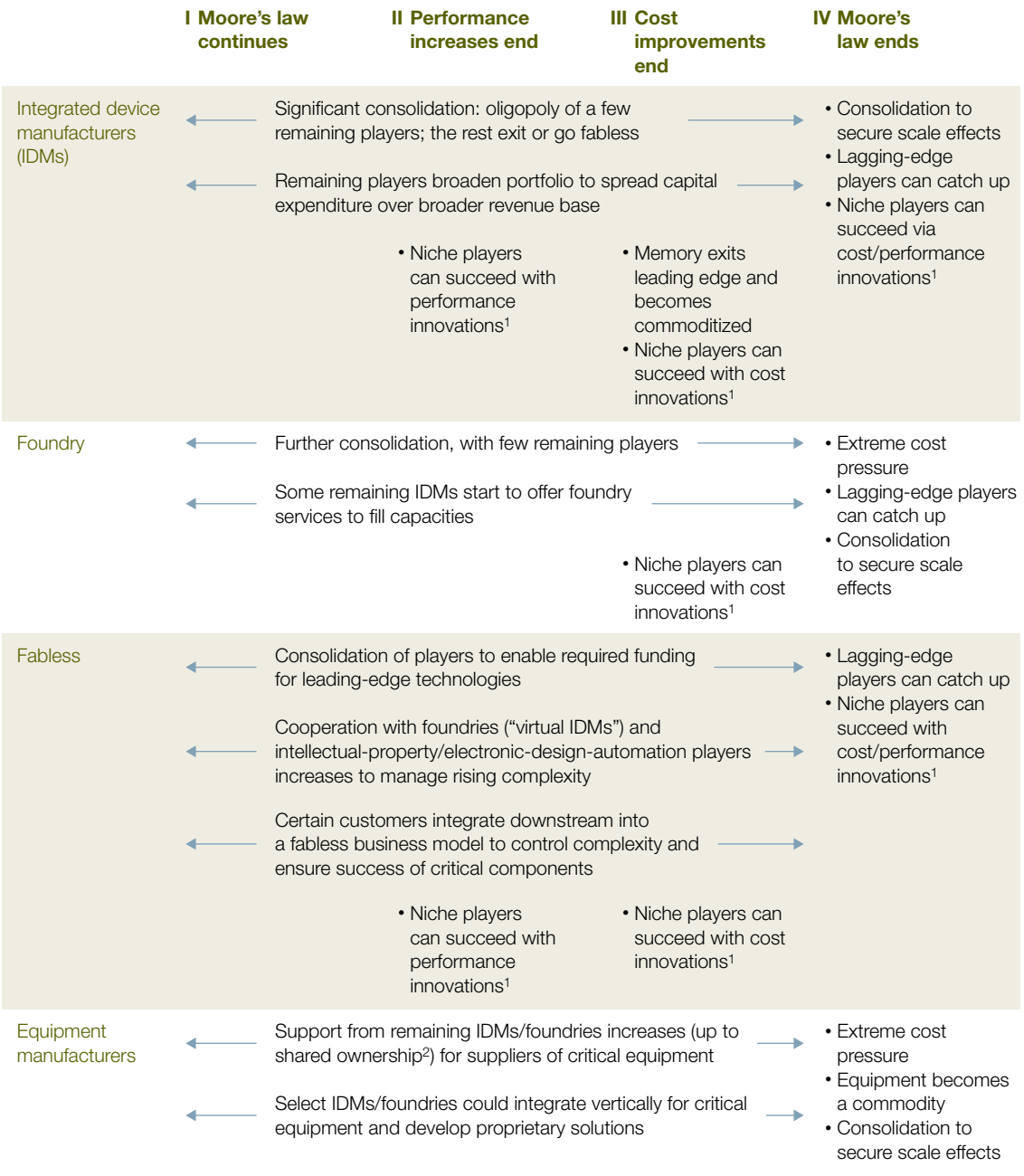
EUV is not production ready because of unsolved technical issues, including the lack of a light source with sufficient power and stability. However, recent developments suggest the industry is moving to make EUV commercially feasible. For instance, ASML, an EUV tool producer, acquired Cymer, which is working on the light-source issue. Additionally, Intel, Samsung, and Taiwan Semiconductor Manufacturing Company have coinvested in ASML to fund EUV development.

A McKinsey survey on the semiconductor business climate index conducted in the fourth quarter of 2012 found that industry experts expect at-scale EUV production to become possible by 2015 or 2016.[1]

[1] McKinsey's survey is a quarterly survey of semiconductor-industry executives to measure the business climate and inquire about selected topics. Results are available only to survey participants.

Exhibit 4

Implications vary depending on a player's place in the value chain.



[1]Other than scaling; examples include chip design or software.
[2]As an "industry foundation," for instance.

A close review of the technologies in development and our scenarios can help to clarify the implications for different players along the value chain.

customer demand probably would shift in important markets such as consumer electronics because end-customer cost declines will cease. The industry itself would remain highly concentrated, and ROIC performance of these companies would drop because of rising capital-spending levels. Finally, the industry's ability to capture value would be at risk because of the disruption of demand.

Each scenario will have different implications for industry players depending on their positions in the semiconductor value chain (Exhibit 4). And if Moore's law does in some way break down, the implications for semiconductor end users will also be significant. One reason for the success of Apple and Samsung has been their ability to provide major increases in performance for the same or lower prices with each new generation of handsets they sell. Were that to end, these players would be forced to seek innovation elsewhere to stimulate demand, such as in additional component technologies or software.

A close review of the technologies in development and our scenarios can help to clarify the implications for different players along the value chain.

Moore's law continues. Under this scenario, both performance and costs would continue to improve through node scaling. The industry would consolidate further, effectively turning into an oligopoly consisting of the few remaining leading-edge players. Only a handful of companies would own leading-edge chip fabs. Some integrated device manufacturers (IDMs) would offer foundry services (meaning they would fabricate the designs of other companies), while others would exit the industry or go fabless. The most advanced IDMs and foundries would probably collaborate closely with equipment manufacturers or might even vertically integrate and develop in-house competence for critical production steps like specific cleaning tools or even lithography equipment. The semiconductor industry would gain increasing market power over its customers, which in turn would lead to greater economic value creation in the sector.

Performance increases end but cost improvements continue. Currently, there is no indication that performance increases will end, but such a state is possible, for example, because of quantum effects as transistors approach atomic scale. In principle, industry dynamics would mimic those under the scenario in which Moore's law continues, but there would be two differences. First, companies would step up their efforts to achieve performance increases through methods other than scaling (for example, by introducing new chip designs and architectures). IDMs and fabless players that would be forced to exit the market if Moore's law continues could

DEEP DIVE

Transitioning to 450mm wafers

Semiconductor companies seek continuous productivity improvements to pay for the increasingly expensive tools and equipment needed to achieve the node-scaling progression underlying Moore's law. Through the years, the industry has made productivity improvements by transitioning to larger wafer sizes; these grew to 300 millimeters (mm) by 2000 from 150mm in the early 1980s. Today, all leading-edge production occurs on 300mm wafers.

The industry's next step could be a switch to 450mm wafers. These would provide a 125 percent increase in area compared with the current 300mm wafer and would lower labor costs, increase the number of dies per wafer, and provide better yields. On the other hand, the cost of equipment will be markedly higher. Analysts estimate that a full-scale 450mm production fabrication plant would run $10 billion to $15 billion. Only a handful of industry players have the financial wherewithal to afford such investments.

Signs of the industry's interest in supporting this advance have become apparent. The Global 450 Consortium, for example, is building a test facility in New York, and Intel has recently invested in 450mm development by ASML.

It is unclear when a 450mm wafer might hit the market. The most recent industry road maps suggest that 450mm volume production will not be available before 2018 or 2020, with the main stumbling block involving lithography processes.

If 450mm wafers become a reality, the advance will have dramatic implications for the industry. Perhaps the most important is the potential for overcapacity. McKinsey analysis indicates that one or two 450mm fabs alone would be sufficient to meet the demand of entire industry segments making products such as central processing units or application processors.

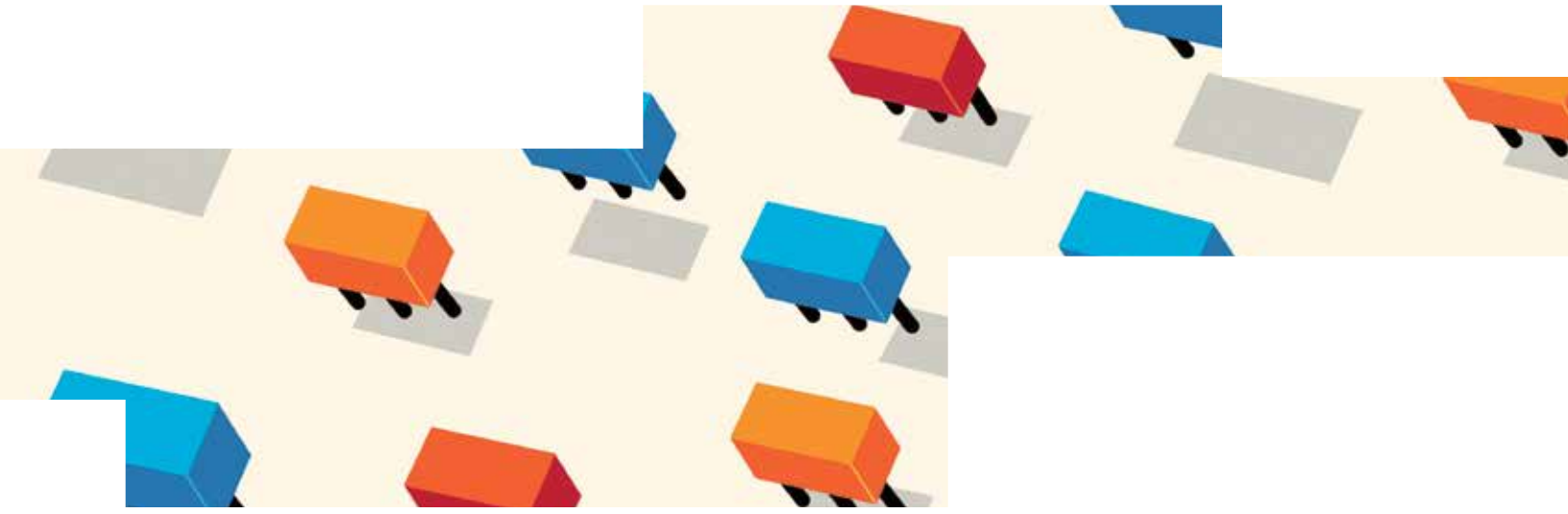
This added production volume could drive players unable to invest in 450mm fabs from the market. These players would have an estimated 30 percent cost disadvantage relative to companies with 450mm fabs. In turn, a switch of leading-edge volume from 300mm to 450mm fabs would free up the 300mm facilities to cannibalize 200mm fabs. As a result, we expect significant overcapacity at the 300mm and 200mm levels if 450mm wafers enter production.

survive in this environment based on such innovations. Second, semiconductor customer industries such as consumer electronics and telecommunications would have to adjust their end-product life cycles because the constant inflow of higher-performing chips would end.

Cost improvements end but performance increases continue. While the cost-related benefits of moving to the next-generation node cease, companies seeking increased performance for its own sake could still gain advantages from further investments. This scenario would likely separate today's leading-edge industry into two parts: the first, consisting of microprocessor units, high-end field-programmable gate arrays, and graphics and wireless chips, would remain on the leading edge. Memory chips, on the other hand, would become commodities.

The dynamics for segments that remain on the leading edge would be similar to those described under the scenario in which Moore's law continues, with two differences. First, to reduce costs, there would be a strong focus on differentiating innovation through means other than scaling, and second, end-product markets would be disrupted because chip prices would stop their continual declines.

Moore's law ends. This is the worst-case scenario, in which both performance and cost improvements would cease. While the overall industry would experience technological commoditization, new elements such as software or design could become differentiating factors. A few large-scale commodity players would dominate, and some niche firms would succeed by offering differentiated products. This scenario would open the door to today's lagging-edge players (or even new entrants), allowing them to catch up to technology leaders on node scaling and to compete successfully using innovations other than scaling. Under this scenario, the equipment employed in semiconductor fabrication would become commodi-



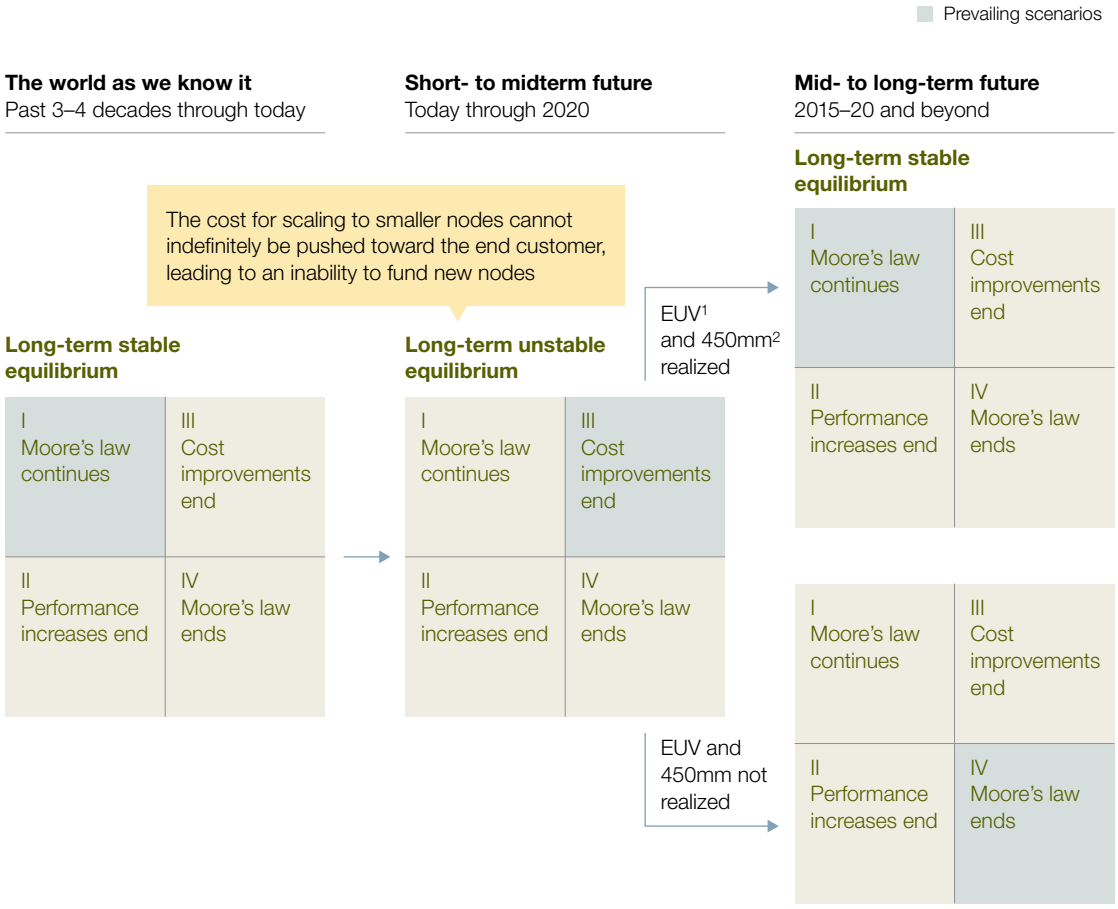
tized, and the industry that produces it would consolidate. Stabilized chip prices and changes in innovation cycles would significantly disrupt many end-customer markets. The semiconductor industry itself would struggle to create significant economic value because of commoditization. One bright spot: the industry's ROIC should improve because capital and R&D spending requirements would slow.

Which scenarios, in what order?

Industry leaders should understand that each of these scenarios could unleash different industry dynamics and that they need to be

Exhibit 5

The industry is moving toward the third scenario, but this won't be stable in the long term.



[1]Extreme-ultraviolet lithography.
[2]450-millimeter wafers.

prepared for each possibility. We believe that the industry is moving toward the third scenario—under which cost improvements end—because of the cost-advantage lag now seen in nodes below the 28nm to 20nm range (Exhibit 5).

In the mid- to long term, however, this scenario would not create a stable industry equilibrium; as a result, two other outcomes become possible. If EUV lithography and 450mm wafer sizes are successful, manufacturers could overcome the cost disadvantages caused by multipatterning, and the industry would likely move back to the first scenario, in which Moore's law continues. Semiconductor road maps currently suggest that the required tools and technologies for EUV will be available by 2015 and for 450mm wafers by 2018. The failure to commercialize these technologies might, over the mid- to long term, result in the end of Moore's law (our fourth scenario).

• • •

Moore's law has guided the global semiconductor industry for nearly five decades, but pressing economic challenges could undercut its impact for at least part of the industry over the short to midterm. The major challenge ahead involves mitigating the potentially negative implications of a missing cost advantage in the near term, while also carefully watching how competitors prepare for the long term. We believe that interesting years lay ahead for the semiconductor industry because the steady evolution the industry historically counted on might be coming to an end.

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