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Taking the next leap forward in semiconductor yield improvement

By prioritizing improvements in end-to-end yield, semiconductor companies can better manage cost pressures and sustain higher profitability. The path forward involves a shift in mind-sets as well as deployment of advanced-analytics solutions.

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As we progress into the digital era, semiconductor manufacturing competition is intensifying, with industry players looking to make productivity improvements while undertaking a record level of M&A activity. Front-end fabs and back-end manufacturers have typically focused transformational improvement efforts on direct and indirect labor-cost reduction, overall equipment effectiveness and throughput increases, material consumption and cost reductions, and global-procurement and spending adjustments. Although lean techniques have been the standard method of achieving productivity gains, many companies—particularly back-end manufacturers—have difficulty sustaining lasting impact.[1] Our experience working in Asia shows that a differentiating factor to effectively manage increasing cost pressures and sustain higher profitability is improving end-to-end yield—encompassing both line yield (wafers that are not scrapped) and die yield (dice that pass wafer probe testing).

Yield optimization has long been regarded as one of the most critical, yet difficult to attain goals—thus a competitive advantage in semiconductor operations. According to the Integrated Circuit Engineering Corporation, yield is "the single most important factor in overall wafer processing costs," as incremental increases in yield significantly reduce manufacturing costs.[2] In this regard, yield can be viewed as being closely tied to equipment performance (process capability), operator capability, and technological design and complexity. Over the years, advances in fab technology such as more efficient air-circulation systems and better operator capabilities, as well as efforts to lessen direct human contact with the production process through the use of automation, have led to a decline in particulate problems.[3] And yet many semiconductor players struggle to implement sustainable yield improvements due to ingrained mind-sets, an insufficient view of data, and isolated efforts as well as a lack of advanced-analytics capabilities.

As devices continue to get smaller and more sophisticated, the effects of Moore's law—that is, the estimation that the number of transistors in a given chip doubles every two years—will continue unabated. Thus in the semiconductor industry, the risks to yield due to process variability and contaminations are ever increasing, as is the importance of continuously improving design and machine capabilities. In this paper, we describe a new approach to changing mind-sets, gathering the right data to inform improvement initiatives, and achieving sustainable yield increases through systemic improvements. We also offer an overview of the impact that advanced analytics can have on semiconductor yield and highlight seven capabilities that semiconductor players can pursue to inform their efforts.

Current perspectives on improving yield

Much has been discussed around the advent of Industry 4.0 tools to improve yield across front-end and back-end manufacturers. Yet without even entering that stage of technological maturity, most semiconductor players still seek to understand yield data by focusing on excursions, percentage, or product—or a combination of the three.

A percentage focus involves a bottom-up approach toward viewing yield percentages, either as an integrated view or by specific process areas. This information is typically highly dependent upon the accuracy of the data captured by operators and made readily available for engineers through manufacturing execution systems.

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Some manufacturers focus on a specific set of products or product families, either by highest volumes or lowest yield performances. Resources are then assigned to solve for the root causes of specific product problems, as a means of prioritizing the company's efforts. This approach requires engineering resources from cross-functional teams, such as equipment, process, product, quality, testing, and, of course, yield.

Excursion—that is, when a process or piece of equipment moves out of preset specifications—can be a significant contributor to yield loss, particularly if it goes undiscovered until after fabrication. An excursion focus can thus be defined as tackling the highest and most obvious sources of yield loss or excursion cases identified from past historical occurrences either in the plant or from customer incidents. The key focus is to ensure the root causes of those yield losses and their potential failure modes are addressed to avoid a repeat occurrence.

These approaches can enable manufacturers to capture, monitor, and control various forms of yield losses—but they may leave other opportunities on the table. To target the highest impact on profitability, semiconductor companies must first translate yield loss into actual monetary value (rather than simply volumes or percentages), enabling them to more effectively direct resources toward solutions across all products and processes. This approach goes beyond a yield-loss focus on specific products or excursion cases to encompass a more end-to-end view. As a result, semiconductor companies can more effectively implement systemic process changes and, particularly given the different cost structures for each product, result in significant and as yet unrealized cost savings.

A new approach to semiconductor yield improvements

To translate yield loss into actual monetary value, a semiconductor company must begin by aligning the language and data used by engineering and finance to gain a better understanding of end-to-end yield. Next, it can use a loss matrix to develop a holistic view of the company's greatest sources of loss; then it can use that data to design more targeted initiatives that will have the biggest impact on increasing yield—and thus on improving the company's bottom line.

Align the language and data of engineering and finance

In our experience with semiconductor manufacturers, there is a consistent disconnect between the engineering and finance functions. Engineers focus on and celebrate gains in percentage yield, but they often overlook the connection between yield and cost. Indeed, the celebrated percentage

increases may or may not lead to any significant impact on the bottom line. Furthermore, many engineering and finance functions use different systems to track yield, which can result in constant disagreements or misalignment between the functions, rendering data less usable by the lack of agreement about which to use as the source of truth.

The first step in ensuring that all functions are aligned in a yield transformation effort is to speak a common language—the cost of poor quality. Using this understanding as a means of alignment immediately proves fruitful for all involved. Not only can engineers and finance personnel understand each other but the ease of translation and communication also extends vertically through the organizational ladder, allowing both ground-level engineers and top-level management to agree on justifications for pursuing initiatives and on progress achieved for successful improvement activities.

To overcome divergent sources of truth, semiconductor companies can construct a cost-of-non-quality (CONQ) baseline that uses cost data from finance as well as engineering (Exhibit 1). For example, finance provides data on standard costs, standard yields, and yearly volumes per product, while engineering provides detailed breakdowns on the nature (reject category) and source (process) of the defects by product. Merging these two views provides a full and readily approachable view of the cost of yield losses.

Exhibit 1 **Cost-of-non-quality (CONQ) calculation can be broken down into three components: volume, standard cost, and yield.**

CONQ calculation breakdown

CONQ total	=	Actual scrap volume	×	Average standard cost per unit	× Average standard yield
Example		• Chips detected as defective • Chips falling into bins allocated for scrap		• Cost per chip increased by expected scrap (yield)	• Expected die yield percentage
Description		• Quantity of scrap attributable to die yield loss, ie, products discarded during production • Scrap quantity measured at process output, reported in enterprise resource planning system		• Average cost per chip, including: — Variable (material) costs — Overhead (including labor) costs — Yield adjustment, ie, additional unit cost due to yield losses	• Percentage of expected yield loss used for standard chip costing, multiplied by the average standard cost per unit, gives the "unyielded" cost, ie, the real cost at input
Not included		**Utilization loss:** Working chips that are unsold and scrapped after six months **Rework:** Defective chips thrown into bins for reprocessing to ideally produce a good chip **Freight costs:** Cost of transportation of wafers from upstream processing			

Engineering must take a step back to see exactly what parts of the process, and specifically what reject categories, lead to the greatest amount of loss.

Develop a holistic, data-driven view of what needs to improve and where

Typically, engineers are dedicated to discrete processes, enabling them to develop deep expertise in a given area and more effectively serve on the line. However, when embarking on a yield transformation, a semiconductor company must develop a holistic view of the manufacturing process. Therefore engineering must take a step back to see exactly what parts of the process, and specifically what reject categories, lead to the greatest amount of loss. While some companies already undertake a product focus to yield losses, an overarching view of the entire manufacturing line is usually not top of mind. Thus, instead of a singular transformation, what usually happens is a lot of the efforts are siloed into individual processes, products, and even pieces of equipment.

A loss matrix enables engineering to map process areas (in a heat map) and reject categories against yield performance of the manufacturing line from start to finish. One manufacturer found that across the eight major steps of its semiconductor production process, the company was losing almost $68 million due to yield losses overall, including almost $19 million during electrical testing alone (Exhibit 2). Engineers can use their technical knowledge of what happens in particular processes to determine why certain reject codes are high within those processes. By also calculating the addressable amount of loss, this heat map view enables the organization to prioritize its focus and allocate resources to the process areas most likely to improve profitability.

In our experience, having this view handy is extremely useful not only to ensure that everyone has a view of what must be addressed and where but also to keep track of what areas have been covered—and which ones are still unexplored. The heat map also enables engineers to take a top-management approach toward the line as a whole, instead of focusing only on their particular process, and reinforces the view that all engineers are responsible for managing quality and yield.

Implement systemic improvements to identify yield loss

Once the biggest loss areas are identified using the loss matrix, it is important to ensure the resulting improvement activities are sustainable; this starts by isolating the products that are the biggest contributors to scrap (Exhibit 3). This per-product analysis ensures that action is taken only on items that have the biggest impact on yield.

Exhibit 2

An example loss matrix illustrates how manufacturers can identify major yield losses by category to help prioritize improvement efforts.

2018 estimated CONQ, USD millions

X Addressable amount Y Targeted savings amount <1.0 1.0–2.0 >2.0

Reject category/ process area	Electrical testing	Tape and reel	Visual inspection	Assembly package 1	Die attach	Pick and place	Assembly package 2	Assembly package 3
Loose dies	3.1 (X 3.1, Y 1.0)	1.0 (X 1.0, Y 0.4)	1.2 (X 1.2, Y 0.3)	-	0.2	2.2 (X 2.2, Y 1.0)	-	0.2
Contamination/ foreign material	1.1 (X 1.1, Y 0.5)	0.3	1.1 (X 1.1, Y 0.4)	2.1 (X 2.1, Y 1.0)	0.4	0.9	-	0.9
Bulge/bubble/wrinkles	-	1.3 (X 1.3, Y 0.3)	-	3.5 (X 3.5, Y 1.5)	1.0 (X 1.0, Y 0.5)	-	-	-
Flux losses	0.7 (X 0.7, Y 0.3)	0.2	-	-	-	-	-	-
Quality reject	-	-	1.1 (X 1.1, Y 0.3)	-	-	2.5 (X 1.5, Y 0.9)	-	-
Previous reject: From upstream	-	0.2	0.9	0.9	-	-	-	-
Broken tile/ceramic crack	0.5	0.3	1.0	1.1 (Y 0.4, Y 0.1)	0.9	0.5	-	-
Insufficient silicone	-	-	1.9 (X 1.5, Y 0.5)	-	0.9	-	1.0 (X 1.0, Y 0.4)	-
Evaluation	0.6	0.4	1.0	-	0.9	0.5	-	-
Contact resistance/ no contact	1.5 (X 1.5, Y 0.4)	-	-	-	-	-	-	-
Tile calibration retesting	3.5 (X 3.5, Y 1.0)	-	0.9	-	-	-	-	-
Minor coverage of assembly package	-	-	-	-	-	-	1.0 (X 1.0, Y 0.3)	-
Other	1.5	0.5	0.9 (Y 0.9, Y 0.2)	-	1.5	1.3	0.9 (Y 0.9, Y 0.3)	-
Remaining long-tail losses	6.2	1.6	0.5	0.3	1.5	1.6	2.0 (X 2.0, Y 1.5)	2.1 (X 2.0, Y 0.1)
Total loss	**18.7**	**5.8**	**10.5**	**7.9**	**7.3**	**9.5**	**4.9**	**3.2**

One manufacturer found that across the eight major steps of its semiconductor production process, the company was losing almost $68 million due to yield losses overall.

Exhibit 3 **Product analysis helps manufacturers gain clarity on the biggest contributors to the overall yield loss and size gap to target.**

Week:

Process 1 target	Process 2 actual	Gap to target	Contribution
85%	81.3%	–10.0%	–10.0%

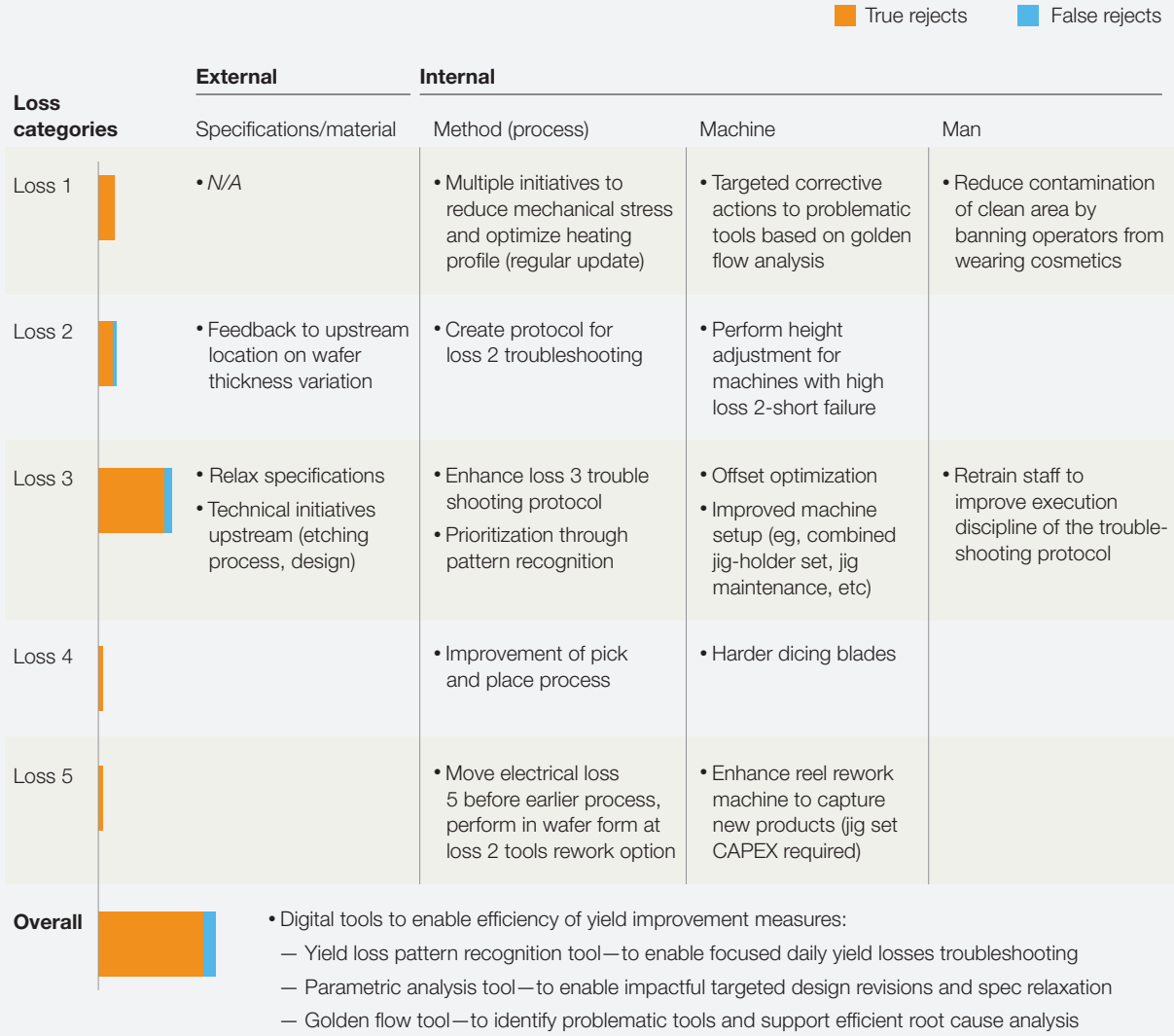
X top products contribute to X% drop of yield (overall gap to target is x.x%, partly positively impacted by parts that are better than target)

Product	Yield	Gap to target	Contribution	% of scrap	% mix	Scrap/mix
Product 1	72%	–18%	–7%	26%	21%	6.4
Product 2	34%	–57%	–8%	21%	11%	8
Product 3	43%	–48%	–7%	17%	9%	7.6
Product 4	68%	–22%	–6%	11%	9%	6.5
Product 5	84%	–6%	–5%	10%	11%	5.8
Product 6	12%	–78%	–6%	10%	6%	8.9
Product 7	88%	8%	5%	9%	11%	5.7
Product 8	73%	–17%	–5%	8%	8%	6.3
Product 9	90%	10%	5%	8%	10%	5.6
Product 10	91%	10%	5%	7%	9%	5.6
Product 11	68%	–5%	–5%	7%	6%	6.5
Product 12	86%	5%	5%	7%	7%	5.8
Product 13	83%	–8%	5%	6%	7%	5.9
Product 14	87%	6%	5%	6%	7%	5.7
Product 15	87%	6%	5%	6%	7%	5.7
Product 16	99%	14%	6%	6%	11%	5.2
Product 17	93%	13%	5%	6%	7%	5.5
Product 18	92%	12%	5%	6%	7%	5.5
Product 19	94%	14%	5%	6%	8%	5.4
Product 20	89%	9%	5%	6%	6%	5.6

As a result, engineers have the detailed insight they need to solve for key themes that drive the particular losses identified by the loss matrix. They can also use a product Pareto analysis to identify the use cases where addressing an issue will solve the most significant, far-reaching problems.

Key improvement themes are generally structured using the traditional "5 Ms" of lean manufacturing—machine, man, material, measurement, and method. While organizing loss categories along these lines, semiconductor companies should also analyze which rejects are true and which are false, as well as discuss what potential cross-functional collaborations may help solve the issue. One manufacturer completed an analysis on four of the Ms (measurement

Exhibit 4 **Key improvement themes are to be identified, evaluated, and structured in close collaboration with the client experts.**



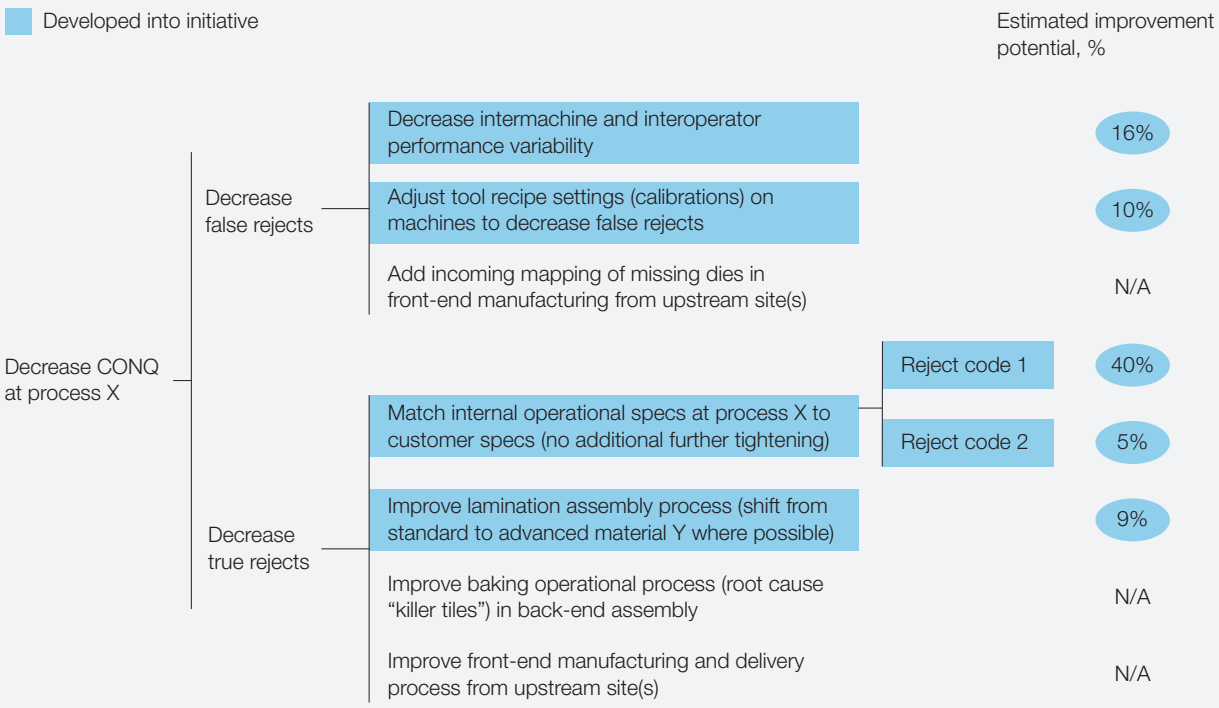
Loss categories	External: Specifications/material	Internal: Method (process)	Internal: Machine	Internal: Man
Loss 1	• *N/A*	• Multiple initiatives to reduce mechanical stress and optimize heating profile (regular update)	• Targeted corrective actions to problematic tools based on golden flow analysis	• Reduce contamination of clean area by banning operators from wearing cosmetics
Loss 2	• Feedback to upstream location on wafer thickness variation	• Create protocol for loss 2 troubleshooting	• Perform height adjustment for machines with high loss 2-short failure	
Loss 3	• Relax specifications • Technical initiatives upstream (etching process, design)	• Enhance loss 3 trouble shooting protocol • Prioritization through pattern recognition	• Offset optimization • Improved machine setup (eg, combined jig-holder set, jig maintenance, etc)	• Retrain staff to improve execution discipline of the trouble-shooting protocol
Loss 4		• Improvement of pick and place process	• Harder dicing blades	
Loss 5		• Move electrical loss 5 before earlier process, perform in wafer form at loss 2 tools rework option	• Enhance reel rework machine to capture new products (jig set CAPEX required)	
Overall				

- Digital tools to enable efficiency of yield improvement measures:
  - — Yield loss pattern recognition tool—to enable focused daily yield losses troubleshooting
  - — Parametric analysis tool—to enable impactful targeted design revisions and spec relaxation
  - — Golden flow tool—to identify problematic tools and support efficient root cause analysis

was not applicable in that case) and sorted out true from false rejects while also developing a sound foundation for improvement initiatives (Exhibit 4).

One finding from the yield loss analysis showed that the manufacturer was experiencing contamination and wrinkle issues at a particular process point. The ensuing problem-solving session identified underlying, systemic issues in the manufacturing process, resulting in four improvement initiatives relating to both true and false rejects (Exhibit 5).

Exhibit 5 **Idea-generation process starts by brainstorming ways to reduce both true and false rejects and focusing on addressable issues.**



Given their cross-functional nature, the machine variability initiatives entailed both internal effort and external involvement. Internally, product, process, and test engineers, quality engineering, and R&D worked together to run the necessary tests and qualifications to ensure the activity had no negative impact on semiconductor quality. Armed with their analysis, engineers could have more meaningful discussions with external vendors about legacy patches to existing equipment and ideas to improve machine performance.

The implementation of these four initiatives reduced contamination rejects for identified products by 90 percent, and wrinkle rejects by 40 percent, and in the long term and gave valuable insight to engineers in both collaborating with third parties as well as ingraining an ownership mind-set.

Impact to a yield engineer's typical day, with the holistic view of yield improvements

Yield engineering resources are typically spent supporting or leading improvement activities across both product and process engineering. At one manufacturer, yield engineers' daily

activities ranged across three main areas—root-cause problem solving of excursions and other critical identified yield losses, cross-functional yield improvement activities and collaborations with other teams, and operational tracking and reporting of yield performances across the fab. By applying a holistic approach toward yield improvements based on the steps described above, a typical day in the life of a yield engineer improved in all three realms.

Root-cause problem solving. The majority of yield engineering resources used to be spent on yield loss analyses and low-yield threshold troubleshooting, for both mature products and new product releases, from product development including buy-off approvals. Due to the yield loss analysis, the manufacturer's yield engineers could shift from a reactive "firefighting" stance on tackling ad hoc requests or manufacturing execution system triggers to solving for root causes of major excursions or other weekly yield losses on the line. Engineers can now identify key losses as per the loss matrix that are unaddressed and start with the one that will have the biggest forecasted impact to the bottom line. Internal problem solving is further strengthened with the help of big data analytics solutions that proactively highlight commonalities or pattern recognition—for example, a particular tool, process group, or even upstream product or process that contributes significantly to yield losses (see sidebar, "The role of advanced analytics in semiconductor yield improvement: Converting data into actions"). Yield solutions can help push efficiency improvements to the team by providing proactive, low-yield threshold warnings and reporting while also improving turnaround time for lot releases.

Cross-functional yield improvements. Previously, resources were spread across multiple projects or initiatives with other engineering teams, with the main task of using analytics to identify the impact of recommended improvements. Armed with end-to-end traceability of yield losses from front end to back end, yield teams benefit from a more granular view of bottom-line impact, reducing the analytical resources needed and allowing for more insights to be shared with the cross-functional team, including R&D, business-unit sales and marketing teams, and front- and back-end managers. Teams can effectively link decisions from customer requirements (either by R&D or business units), down to bottom-line impact on front-end and back-end expected yield losses, to identify systemic root causes cutting across processes, reject categories, or products. This capability helps yield engineers be more precise in identifying which teams (product or process engineers) are needed and to prioritize which initiatives they ought to invest most of their time. From an efficiency improvement and workload-reduction perspective, teams can better rationalize meeting participation.

Yield engineers are further empowered with data to highlight potential opportunities to implement more yield gains by aligning or relaxing internal specifications, without affecting customer demand or satisfaction. Transparency enables teams across the value chain to collaborate around more data and push initiatives to be more fact based and prioritize resources to maximize profitability.

Yield performance tracking and reporting. For both mature and new unreleased products, yield engineers have shifted from daily or weekly yield percentage monitoring to more continuous monitoring thanks to the capabilities of the loss matrix. Performance baselines and improvements can be tracked and reported either in the form of the loss matrix, or with the

help of analytical yield solutions. Teams can now visualize the distribution of key forecasted shifts in yield losses as measured by monetary impact, which helps prioritize the next wave of improvement initiatives. Reporting is more mutually exclusive and collectively exhaustive than previously limited reporting by process and integral yield percentages.

The role of advanced analytics in semiconductor yield improvement: Converting data into actions

As noted by the CEO of advanced-analytics company Motivo Engineering, "Each fab has thousands of process steps, which, in turn, have thousands of parameters that can be used in different combinations. With so many factors in play, we see a lot of chip failures or defects."[4] Given its complexities, traditional quantitative analysis wouldn't help fabs uncover all improvement opportunities, resulting in a lengthy process of root issue discovery—and thus massive yield losses.

For that reason, the use of advanced analytics offers a new paradigm for yield improvement in the semiconductor industry. Indeed, the nature of manufacturing complexity means there is a big difference between insights from traditional quantitative analysis and those from advanced analytics. Furthermore, semiconductor manufacturing is in a unique position compared with other industries to reap the benefits of advanced analytics given the massive amount of data embedded in fabs' highly automated and sensor-laden environment. Fabs can benefit from yield analytics through three key levers:

- *Early defect detection and root cause identification.* Advanced-analytics tools can help uncover issues much faster and in much greater detail, leading to faster root cause identification. This benefit is greater when we try to uncover root causes of low- and medium-frequency errors, which are difficult to detect using traditional analytics.

- *Improved value-added time for engineers.* At one organization, for example, data pulling and analysis in line maintenance activities can take up more than triple the time required than if data infrastructure and interface are well designed. This situation represents an opportunity to free up engineers' time to focus instead on core issues and production design solutions.

- *Powerful tool for past learning and continuous improvement.* Machine-learning algorithms, a well-organized data lake, and the appropriate tools allow fabs to accumulate learning from past experiences and enable continuous improvement. Whereas the traditional approach eliminates defects by adjusting multiple parameters, which helps with

the current batch, it fails to offer any insight into the root cause of the problem—meaning it is likely to be repeated in future batches.[5]

Identify core analytics capabilities that can improve yield

Seven core analytics capabilities are important in yield management solutions: monitoring and reporting, parametric analysis, correlation analysis, golden flow analysis, equipment optimization, pattern recognition, and event analysis.

- *Monitoring and reporting* is the most basic among the capabilities—but also one of the most important. This process refers to trend charts, histograms, Pareto analysis, proactive reporting and notification, and enhanced statistical process control, all of which enable enhanced performance management of the manufacturing process. These tools and processes enable data to be managed and reported by the engineers so it's most beneficial to their target audience, be they process engineers, managers, or third parties such as customers.

- *Parametric analysis* refers to testing how product parameters are distributed at performance testing and inspections and comparing these findings to product development's specification limits. This analysis ultimately aims to enable the optimization of specifications—tight enough to ensure good quality, but also reasonable enough to prevent unnecessary over- or under-rejection.

- *Correlation analysis* finds correlations between test parameters at earlier stages versus final inspections. This assessment aims to maximize final product performance and help manage end-to-end yield by adjusting test parameters depending on how they correlate with testing results, either electrical or visual test parameters.

- *Golden flow analysis* is a crucial analytical capability to determine tool commonality and identify which tools are performing at optimal levels—and which are not. This data helps with both tool matching and ensuring that production is as high yield and efficient as possible, maximizing throughput and optimizing manufacturing flow (see sidebar "Case study: Golden flow analysis in action").

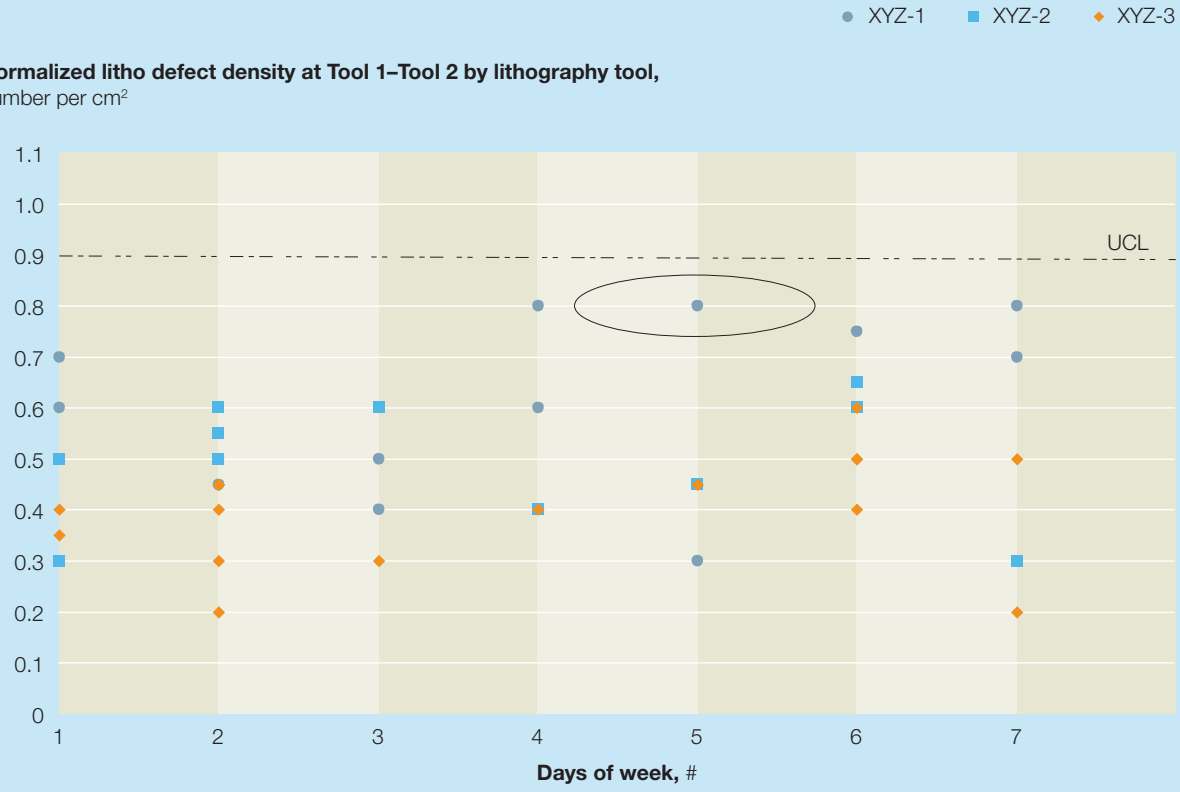
- *Equipment optimization* as an analytical capability refers to how software can perform predictive analyses to determine potential issues before they occur. This ability is closely linked to predictive maintenance and aims to avoid yield loss by tackling predictable tool variation and necessary parameter tuning.

- *Pattern recognition* is about looking at the distribution of parameter patterns across wafer maps and connecting the findings to equipment, manufacturing trends, and correlations with process and test parameters. With this capability, live feedback can be given to engineers so tools and process parameters can be adjusted to reduce yield loss (for more, see sidebar "Case study: Using analytics to reduce losses").

Case study: Golden flow analysis in action

Golden flow analysis helps identify bad actors and golden tools in situations where trends are unclear. At one manufacturer, the analysis detected that a specific tool (XYZ-1), which was one of three tools in the same class and configuration, was experiencing an uptick in normalized defect density across different layers over a seven-day period (exhibit). The uptick had not surpassed the upper control limit (UCL), so without the analysis there would have been no indication of a problem until after it got worse. The advanced warning of increased defect density allowed the manufacturer to take down the tool for investigation, repairs, or calibration interventions.

Exhibit **Commonality analysis helps to identify low-performing and golden tools in situations where trends are unclear.**



- *Event analysis* entails studying production events, such as maintenance and supply changes, to discover their effect on yield. Identifying root causes for quality shifts or parametric surges can be done by tying them to the occurrence of various events on the manufacturing floor.

Case study: Using analytics to reduce losses

One manufacturer developed a false-reject estimator analytics tool for final inspection equipment to help the fab detect and estimate sizes of false rejects based on a pattern recognition algorithm. The algorithm provides a daily, automated report of false rejects at tool and part number (product) levels, enabling a focused effort to tackle problems in a timely manner by comparing with manual estimation and monitoring on a monthly basis. This approach reduced losses from material wastes and customer quality issues while enhancing overall capacity (for example, dice output per day).

Undertake key enablers to overcome typical challenges in implementing yield analytics

Well-organized data integration and interface. Data pull and cleaning (that is, the creation of a data lake) are important steps in deploying analytics. Despite the richness of data gathered through highly automated and sensor-laden systems in fabs, data quality is usually a challenge in implementing analytics software or using data for analysis; for example, different product families have different data formats and complex production processes. The important step is to get individuals with a strong technical knowledge of data and database optimization to create the right data infrastructure to enable scale-up of analytics solutions.

Right organization setup to take data insights to fast action and feedback loop. Converting data and insights into actions is among the most critical steps—and challenges—to capture benefits from analytics. In particular to yield, issues always cross sites and require end-to-end collaboration to get breakthrough results. The key to success is to have effective yield tracking and a platform to enable collaboration and action (for more, see sidebar "Case study: Feedback loop finds costs savings").

Case study: Feedback loop finds cost savings

One semiconductor player operating across regions in Asia and America set up a cross-site yield project management office (PMO) to facilitate end-to-end yield monitoring and speed up the feedback loop. Along with development of four analytical tools and a performance management dashboard, this yield PMO has delivered 10 percent yield improvement and identified and implemented $12 million cost savings opportunity within six months.

Partnerships with technology and analytics vendors. As our colleagues have noted, many analytics and machine-learning vendors believe that semiconductor companies prefer to

develop solutions in-house,[6] which discourages them from building strong relationships with other semiconductor players. In reality, active partnerships with analytics vendors will help increase the speed of building analytics capabilities for fabs. Given the fast-changing environment and highly specialized capability in analytics, ongoing collaboration and partnership will help semiconductor players stay on the cutting edge and employ solutions that enhance in-house capability.

For semiconductor companies, the successes of effective yield improvement lead not only to increased profitability but also to better organizational health as a whole. Our experience points to three central key pillars that make yield transformations successful:

Aligning the language and data of engineering and finance. Looking at yield percentages only provides one view of the situation; engineering and finance alike must align on using the cost of poor quality as the method for understanding and guiding the direction of the company's yield improvement efforts. Collaboration on the creation of a CONQ calculation can ensure that improvement initiatives are based on a viable foundation of data and collaboration.

Develop a holistic, data-driven view of what needs to improve and where. Work on yield can often be siloed due to how manufacturing organizations are structured. Using the loss matrix and analytical solutions—where costs can be easily viewed by processes, reject codes, or products—allows engineers and managers to gain a better view of the health of the entire manufacturing process, from R&D through wafer fabrication and die packaging, to push improvement efforts to the right areas. This view also gives engineers and managers a chance to track what areas they are already tackling, as well as what areas have yet to be explored.

Implement systemic improvements. Yield improvements should address excursion cases—but more important, they should also tackle the baseline yield. By setting up discussions where engineers can explore historic causes of yield loss, new levers can be discovered that will increase overall yield performance for a certain product or process. There can also be situations where certain losses are tolerated simply because they have historically been seen as acceptable. Focusing on standout issues of yield loss, as well as working to continuously improve the baseline yield percentage as a whole, leads to more sustainable yield improvement.

[1] For more, see Koen De Backer, Matteo Mancini, and Aditi Sharma, "Optimizing back-end semiconductor manufacturing through Industry 4.0," February 2017, McKinsey.com.

[2] "Yield and yield management," in *Cost Effective IC Manufacturing,* Integrated Circuit Engineering Corporation, Scottsdale, AZ: 1997.

[3] Jim Handy, "What's it like in a semiconductor fab?", *Forbes,* December 19, 2011, forbes.com.

[4] For more, see "Optimizing back-end semiconductor manufacturing through Industry 4.0," McKinsey.com.

[5] "Yield and yield management," in *Cost Effective IC Manufacturing,* Integrated Circuit Engineering Corporation, Scottsdale, AZ: 1997.

[6] "Reimagining fabs: Advanced analytics in semiconductor manufacturing," March 2017, McKinsey.com.

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